PIC Peripherals

Dr. Altaf Osman Mulani
E&TC Department
SKN SINHGAD COLLEGE OF ENGG., KORTI, PANDHARPUR

Course Outcomes

Course Name	**:Microcontrollers & Applications**	**Course Code:**	**: ET312**
Class	**:Third Year B.Tech.**	**Semester**	**: I**
Academic Year	**:2022--23**	**Subject Teacher**	**: Dr. A. O. Mulani**

CO No.	Course Outcome Statements	Cognitive Level
ET312.1	To recognize the fundamental features and operation of contemporary microcontroller	Remember, Understand
ET312.2	To illustrate the hardware interfacing.	Understand, Apply, Analyze, Create
ET312.3	To discuss the fundamentals of CISC and RISC Microcontroller architectures	Remember, Understand
ET312.4	**To discuss various core and peripheral features in microcontroller family**	**Remember, Understand**
ET312.5	To demonstrate the programs in assembly language and C language for microcontrollers	Understand, Apply, Create

ADCON0 register (address 1FH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	**00**	FOSC/2
0	**01**	FOSC/8
0	**10**	FOSC/32
0	**11**	FRC (clock derived from the internal A/D RC oscillator)
1	**00**	FOSC/4
1	**01**	FOSC/16
1	**10**	FOSC/64
1	**11**	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits

000 = Channel 0 (AN0)
001 = Channel 1 (AN1)
010 = Channel 2 (AN2)
011 = Channel 3 (AN3)
100 = Channel 4 (AN4)
101 = Channel 5 (AN5)
110 = Channel 6 (AN6)
111 = Channel 7 (AN7)

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:
1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

ADCON1 register (address 9FH):

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.

0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 5-4 **Unimplemented:** Read as '0'

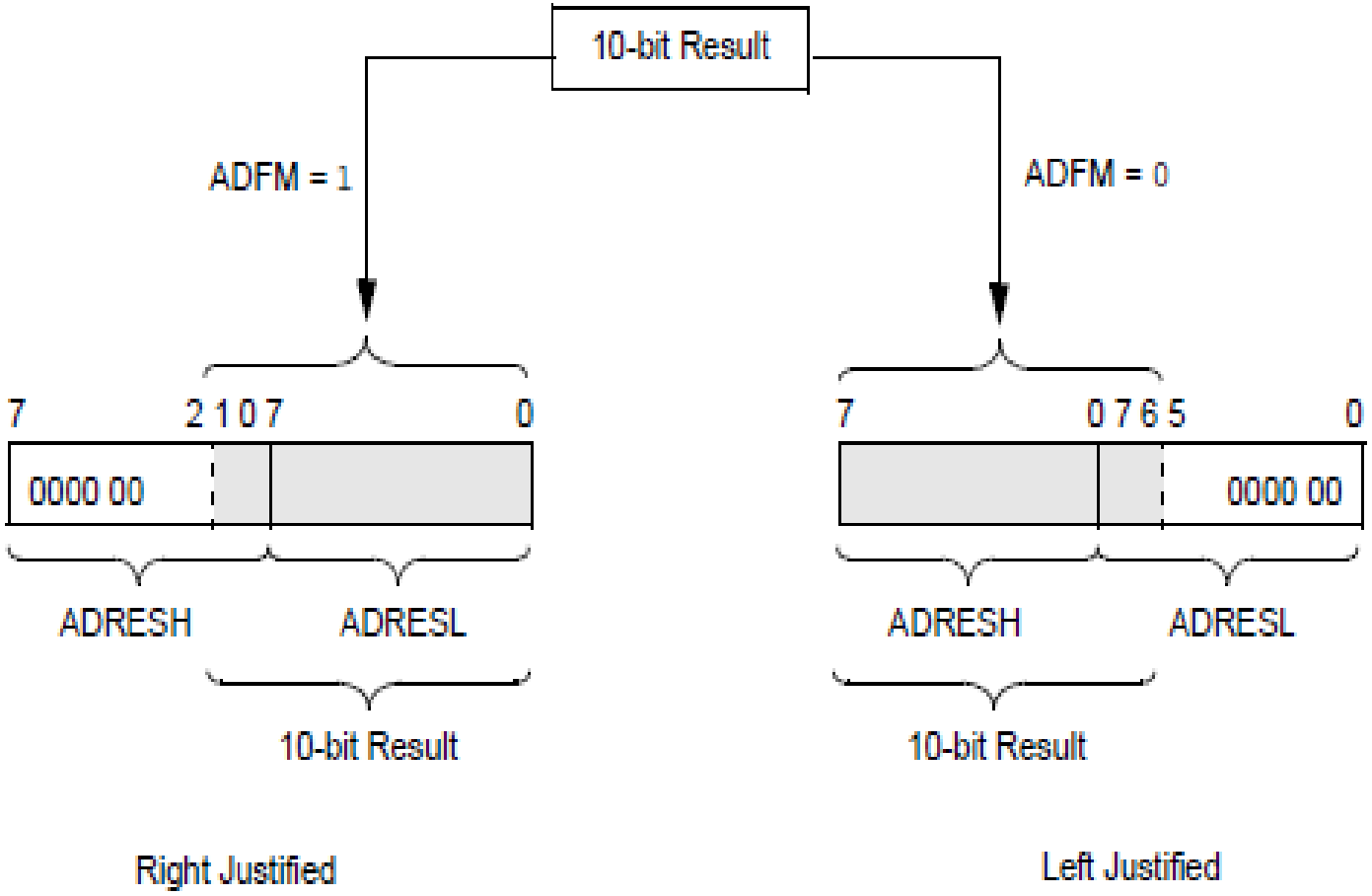
bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references

A/D RESULT JUSTIFICATION



ADC Conversion:

Follow these steps A/D Conversion:

1. Configure the A/D module:
   - Configure analog pins/voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set PEIE bit
   - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
   - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete.
6. Read A/D Result register pair (ADRESH:ADRESL), clear bit ADIF if required.

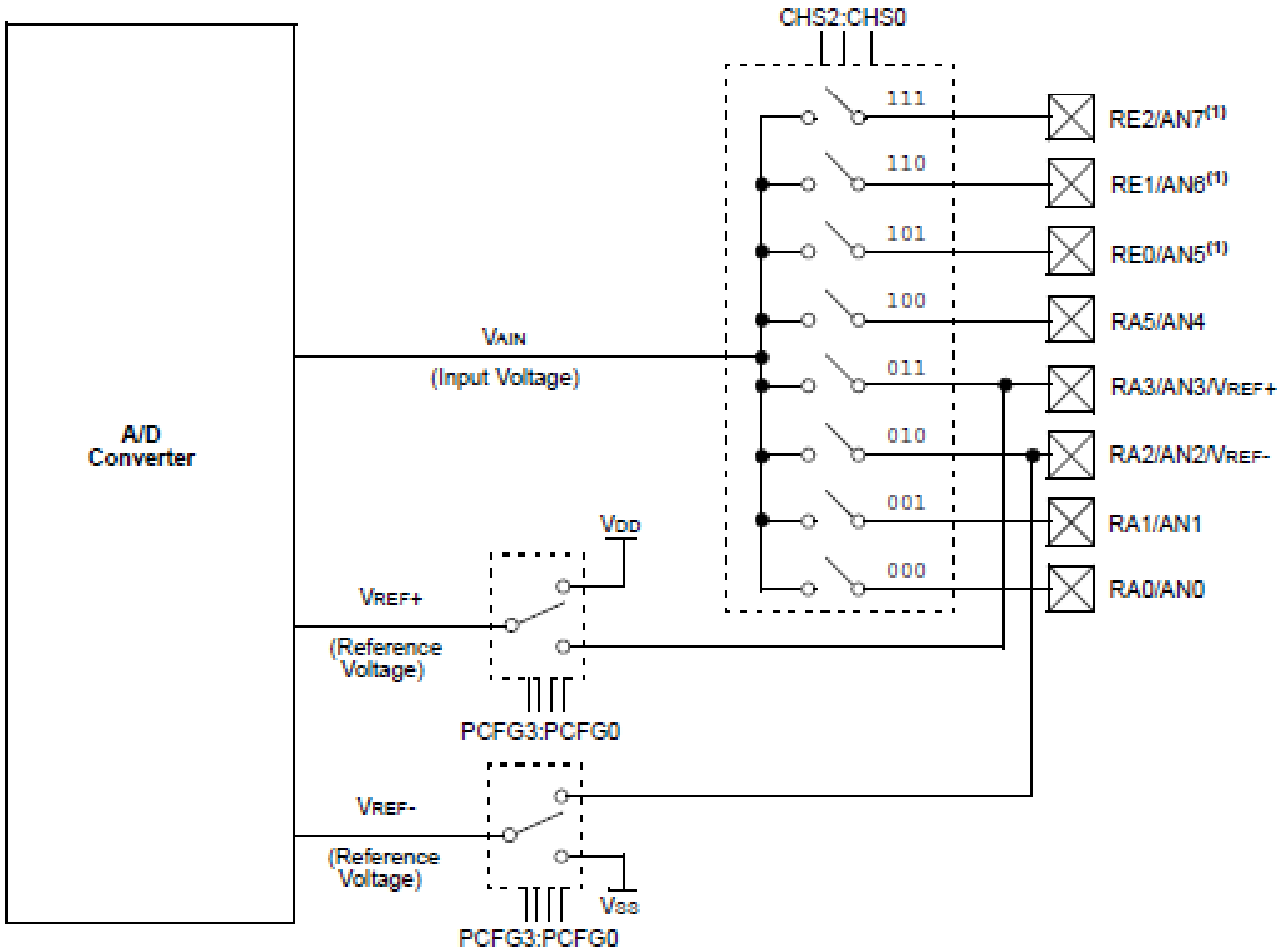
```
#INCLUDE<P16F877A.INC>
R0 EQU 20H
    BSF STATUS,RP0
    MOVLW 80H
    MOVWF ADCON1
    MOVLW 3FH
    MOVWF TRISA
    MOVLW 07H
    MOVWF TRISE
    CLRF TRISB
   CLRF TRISD
   BCF STATUS, RP0

    MOVLW 81H
    MOVWF ADCON0
A1:BCF PIR1,ADIF
    BSF STATUS,RP0
    BSF INTCON,GIE
    BSF INTCON,PEIE
    BSF PIE1,ADIE
    BSF ADCON0,GO

A2:DECFSZ R0
    GOTO A2

A3:BTFSC ADCON0,GO
    GOTO A3
F0:MOVF ADRESH,W
    MOVWF PORTB
    MOVF ADRESL,W
    MOVWF PORTD
    RETURN
END
```

ADC

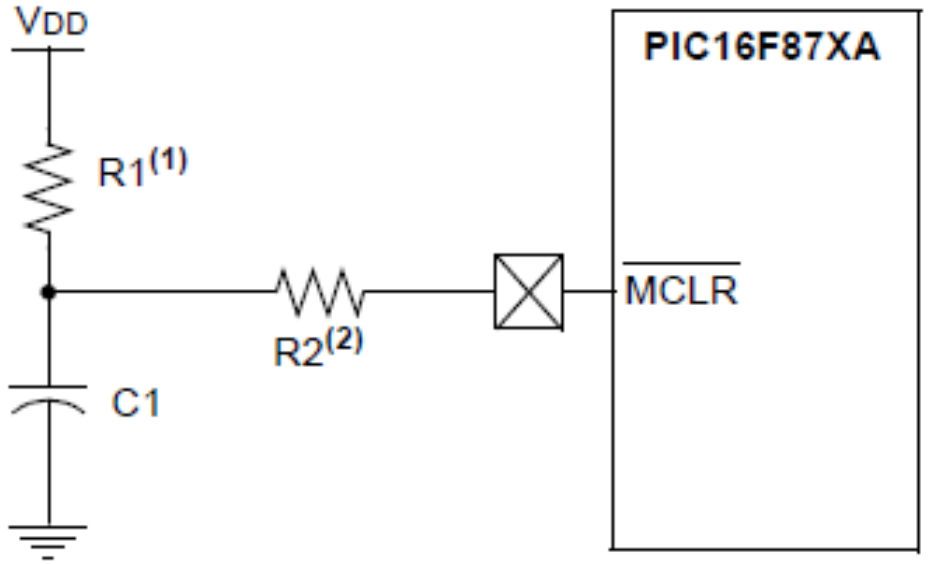

A/D
Converter
CHS2:CHS0
111
110
101
100
011
010
001
000
RE2/AN7(1)
RE1/AN6(1)
RE0/AN5(1)
RA5/AN4
RA3/AN3/VREF+
RA2/AN2/VREF-
RA1/AN1
RA0/AN0
VAIN
(Input Voltage)
VDD
VREF+
(Reference
Voltage)
PCFG3:PCFG0
VREF-
(Reference
Voltage)
VSS
PCFG3:PCFG0

Types of Oscillator

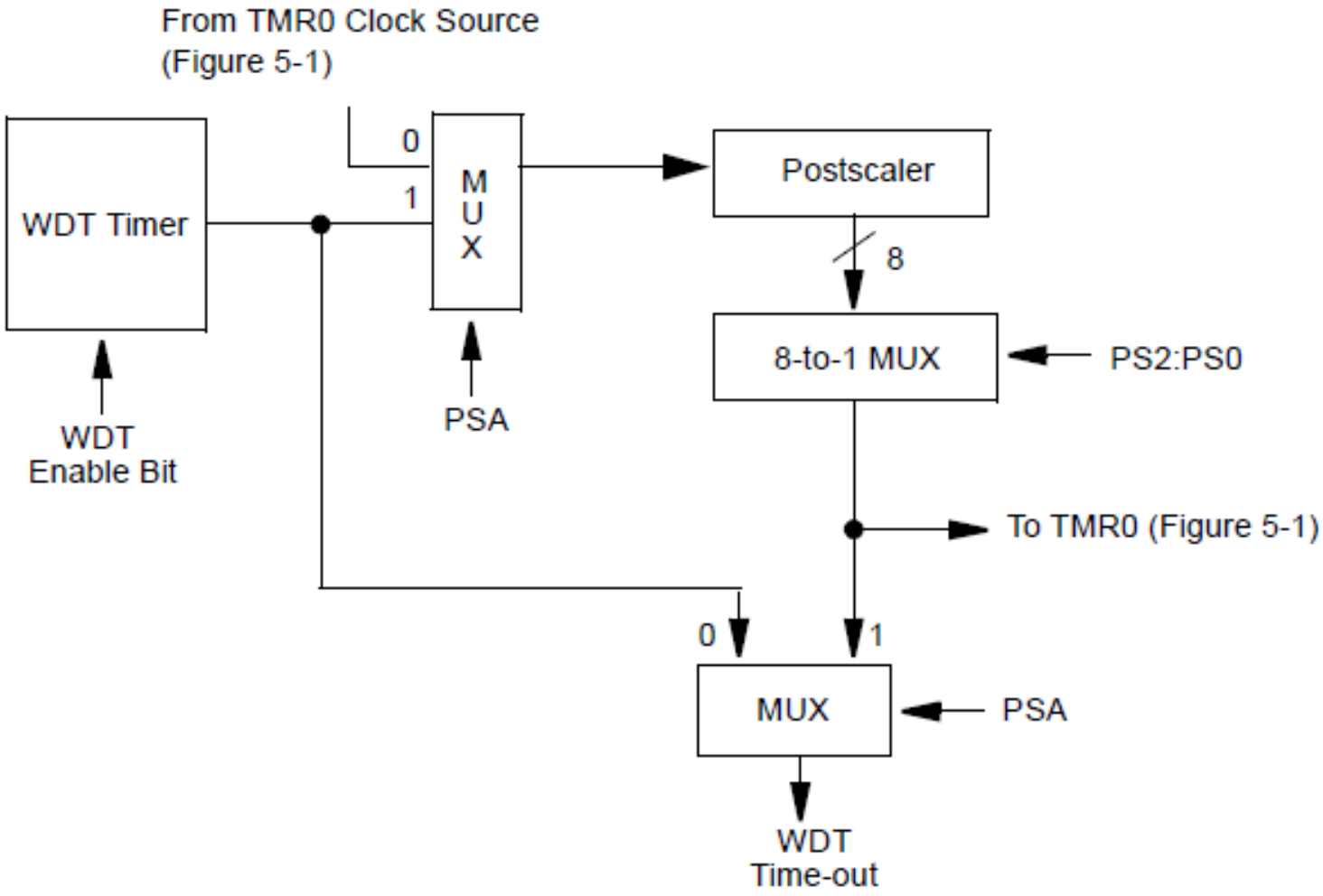
- PIC16F877A can be operated in four different oscillator modes.
- The user can program two configuration bits (FOSC1 and FOSC0) to select one of these four modes:
  - LP Low-Power Crystal (5 – 200 KHz)
  - XT Crystal/Resonator (100 KHz – 4 MHz)
  - HS High-Speed Crystal/Resonator (4 – 20 MHz)
  - RC Resistor/Capacitor (0 – 4 MHz)

Types of reset

- Power On Reset (POR)



Watchdog Timer



Note: PSA and PS2:PS0 are bits in the OPTION_REG register.

Watchdog Timer

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Config. bits	(1)	BODEN(1)	CP1	CP0	$\overline{\text{PWRTE}}$(1)	WDTE	Fosc1	Fosc0
OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

PIE1 Register

PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

PSPIE: Parallel Slave Port Read/Write Interrupt Enable bit

1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt

ADIE: A/D Converter Interrupt Enable bit

1 = Enables the A/D converter interrupt
0 = Disables the A/D converter interrupt

RCIE: USART Receive Interrupt Enable bit

1 = Enables the USART receive interrupt
0 = Disables the USART receive interrupt

TXIE: USART Transmit Interrupt Enable bit

1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

SSPIE: Synchronous Serial Port Interrupt Enable bit

1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

CCP1IE: CCP1 Interrupt Enable bit

1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

TMR2IE: TMR2 to PR2 Match Interrupt Enable bit

1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

TMR1IE: TMR1 Overflow Interrupt Enable bit

1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

PIR1 Register

PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF

PSPIF: Parallel Slave Port Read/Write Interrupt Flag bit
1 = A read or a write operation has taken place (must be cleared in software)
0 = No read or write has occurred
ADIF: A/D Converter Interrupt Flag bit
1 = An A/D conversion completed
0 = The A/D conversion is not complete
RCIF: USART Receive Interrupt Flag bit
1 = The USART receive buffer is full
0 = The USART receive buffer is empty
TXIF: USART Transmit Interrupt Flag bit
1 = The USART transmit buffer is empty
0 = The USART transmit buffer is full
SSPIF: Synchronous Serial Port (SSP) Interrupt Flag bit
1 = The SSP interrupt condition has occurred (must be cleared in s/w)
0 = No SSP interrupt condition has occurred

CCP1IF: CCP1 Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred

0 = No TMR1 register compare match occurred

TMR2IF: TMR2 to PR2 Match Interrupt Flag bit

1 = TMR2 to PR2 match occurred

0 = No TMR2 to PR2 match occurred

TMR1IF: TMR1 Overflow Interrupt Flag bit

1 = TMR1 register overflowed (must be cleared in software)

0 = TMR1 register did not overflow

PIE2 Register

—	CMIE	—	EEIE	BCLIE	—	—	CCP2IE
bit 7							bit 0

CMIE: Comparator Interrupt Enable bit
1 = Enables the comparator interrupt
0 = Disable the comparator interrupt

EEIE: EEPROM Write Operation Interrupt Enable bit
1 = Enable EEPROM write interrupt
0 = Disable EEPROM write interrupt

BCLIE: Bus Collision Interrupt Enable bit
1 = Enable bus collision interrupt
0 = Disable bus collision interrupt

CCP2IE: CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

PIR2 Register

—	CMIF	—	EEIF	BCLIF	—	—	CCP2IF
bit 7							bit 0

CMIF: Comparator Interrupt Flag bit
1 = The comparator input has changed (must be cleared in s/w)
0 = The comparator input has not changed

EEIF: EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in s/w)
0 = The write operation is not complete or has not been started

BCLIF: Bus Collision Interrupt Flag bit
1 = A bus collision has occurred in the SSP when configured for I2C Master mode
0 = No bus collision has occurred

CCP2IF: CCP2 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in s/w)
0 = No TMR1 register capture occurred

Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in s/w)
0 = No TMR1 register compare match occurred